

# SVPWM for two Legged Three Phase Multilevel Inverters – a Simplified Approach on 16 Bit Microcontroller Platform

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**ABSTRACT**— The paper brings out the observation that the space vector representation of four switch three phase inverter. It is used to develop a simple and generalized Space Vector Pulse Width Modulation (SVPWM) algorithm for two legged multilevel inverters. The space vectors of any n-level inverter can be generated from the vectors of 2-level inverter using simple addition operation and doesn't use any look up tables. The simple addition operation used for the generation of space vectors of n-level inverter is also used to generate the inverter switching states of the corresponding vectors. The proposed algorithm is a generalized algorithm and can be extended to any n-level inverter configuration without any computational complexity. The validation of the algorithm through simulations in MATLAB/SIMULINK and experimental in PIC24HJ128GP310 microcontroller has been carried out for 3-level inverter configurations for which the results are also presented.

**KEYWORDS**— Two legged multilevel inverters, Four switch three phase inverter [FSTPI]topology, Space vector pulse width modulation [SVPWM].

## I. INTRODUCTION

Multilevel Inverter Technology has emerged as a powerful technique in the area of medium voltage high power applications [1],[2]. Multilevel inverter synthesizes desired output voltage from multiple levels of dc voltages. As the number of voltage level increases the harmonic content of output voltage waveform decreases significantly [2]. Multilevel inverters gained more attention in recent years due to its inherent advantages of high Voltage-Ampere rating and good harmonic rejection capabilities. The requirement of more number of semiconductor switches is the major disadvantage of multilevel inverters. Although low voltage rated switches can be used in a multilevel inverter, each switch requires a related gate drive protection circuits. Hence the overall system becomes more complex and expensive. In addition increased number of switches increases the switching losses and electromagnetic interference (EMI). So in many practical applications for efficient operation of multilevel inverters, reduction in the number of power semiconductor switches of the inverters is drawing significant research attention [1-2]. The four-switch three-phase inverter [FSTPI] topology is one of the techniques to reduce the number of switches in the inverter [3]. In comparison to the conventional three-phase Voltage Source Inverter with six switches, four-switch three-phase inverter uses only two legs, with a pair of complementary power switches in each leg. Reduction in the number of power switches, switching driver circuits, conduction losses and total price are the main features of FSTPI topology. The two legged 2-level inverter configuration is referred to as the four switch topology in literature. Fig.1 shows the extension of the four switch inverter topology to 3-level inverter configuration.

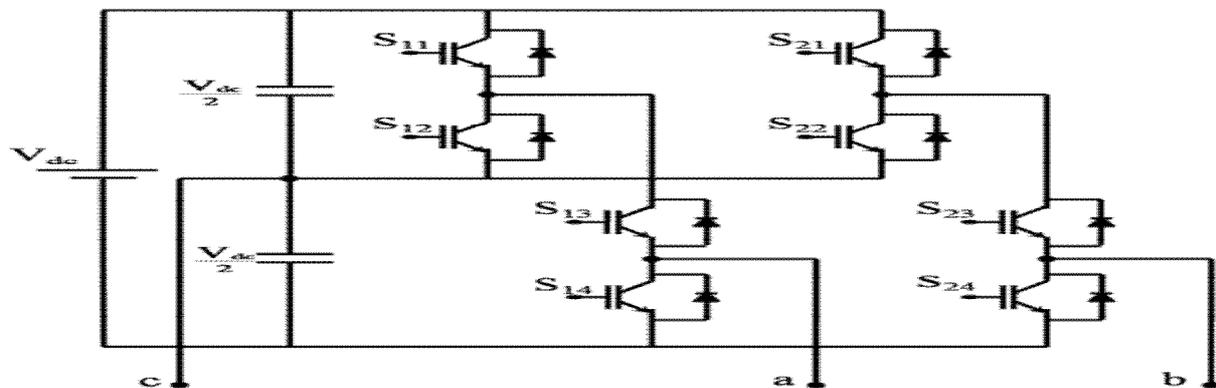


Fig. 1: Circuit of a two legged 3-level inverter

For efficient operation of multilevel inverters various pulse width modulation (PWM) techniques are used [4]-[6]. The most popular PWM techniques used in multilevel inverters are Sine-Triangle PWM (SPWM) and Space Vector PWM (SVPWM). In multilevel SPWM, PWM signal is generated by comparing sine wave with a number of levels shifted triangular carrier signals [7],[8]. For an 'n level' inverter is used, 'n-1' carriers are used. SVPWM involves approximating the instantaneous reference vector by switching the three nearest inverter voltage vectors. With the advanced digital signal processors SVPWM technique became the most popular PWM method and it utilizes the space vector concept for generating the duty cycle of the switches. In SVPWM scheme, the reference voltage space vector is synthesized by switching the three nearest voltage space vectors from among the inverter voltage vectors [9]-[15]. SVPWM technique has many advantages compared to the SPWM such as better dc voltage utilization, reduced harmonics, reduced switching losses and easy implementation. The implementation of SVPWM involves the following steps: 1) identification of the sector in which encompasses the tip of reference space vector, is done by using coordinate transformation of the reference vector to two dimensional coordinate system; 2) determination of the three nearest switching vectors and compute the switching time duration of each of these switching voltage space vectors. The SVPWM generation for three legged multilevel inverters utilizing the inherent fractal structure is explained in [14], [15]. There has been significant work in the area of Space vector PWM for FSTPI but the extension to multilevel inverter configuration is yet to be explored [16]-[21].

The paper explores the possibility of extending the SVPWM generation for FSTPI topology to multilevel inverter configurations. The paper begins with the space vector representation of two legged multilevel inverters and brings out the observation that the voltage space vector representation of a two legged multilevel inverter also has an inherent fractal structure. The inherent fractal structure is utilized in the paper to propose a simple and generalized algorithm to generate SVPWM for any multilevel inverter configuration without any computational complexity. The voltage space vectors of higher level two legged inverters are obtained from the voltage space vectors of equivalent 2-level inverter using simple arithmetic operations. The paper presents the simulation results of the algorithm implemented in MATLAB/SIMULINK for 3-level inverter configurations.

## II. SPACE VECTOR REPRESENTATION OF TWO LEGGED MULTILEVEL INVERTER

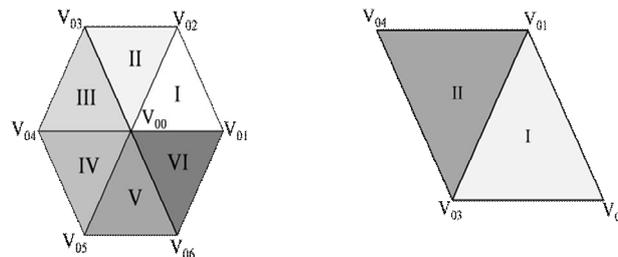


Fig. 2: Voltage space vector locations of (a) conventional three phase inverter (b) two legged three phase 2-level inverter

SVPWM technique utilizes the space vector concept for computing the duty cycle of the semiconductor switches in the inverter. SVPWM generation involves synthesizing the reference voltage space vector by switching the three nearest voltage space vectors. The three instantaneous phase voltages is represented as a space vector in the  $(\alpha, \beta)$  plane. Voltage space vector locations of a conventional three phase inverter are shown in Fig.2 (a). The space vector representation of conventional 2-level inverter has six triangular regions, results from the eight switching vectors, numbered I-VI in Fig.2(a). Fig.2 (b) shows the voltage space vector representation for a two legged three phase 2-level inverter. It may be noted from Fig.2 that the SVPWM generation for the two legged inverter is greatly simplified due to the inherent advantage of only two triangles for encompassing the reference vector against six triangles for the conventional three phase inverter. The advantage of lesser triangles further simplifies the generation of SVPWM for higher level inverter configurations. The two legged inverter configuration is the four switch inverter topology referred to in literature. The four switch inverter topology has four inverter voltage vectors located at the vertices of the parallelogram which be divided into two equilateral triangles numbered I and II in Fig.2(b).

In addition to the inherent advantage of reduced number of triangles, the paper brings out the observation that the voltage space vectors of any  $n$  level inverter can also be generated from the voltage space vectors of an equivalent 2-level inverter. Fig.3 shows the space vector representation of 3-level two legged inverters and the space vector representations of the three phase inverter for 3-level operation. The equilateral triangle formed by the three nearest voltage vectors as vertices known as a sector. Consider the space vector representation of 2-level two legged inverter [Fig.2(b)]. It consists of two sectors; where sector I is formed by the vectors located at  $V_{01}, V_{02}$  and  $V_{03}$  sector II is formed by the vectors located at  $V_{01}, V_{03}$  and  $V_{04}$ . It may be noted from Fig.2(b) and Fig.3(b) that the voltage space vector locations  $V_{01}, V_{02}, V_{03}$  and  $V_{04}$  are in the same locations in both 2-level and 3-level configurations. Also 3-level inverter has five additional voltage vectors located at  $V_{11}, V_{12}, V_{13}, V_{14}$  and  $V_{00}$  compared to the 2-level configuration. Consider the sector I of the 2-level inverter. As in Fig.3(b) in the case of 3-level inverter, this region has three additional voltage space vectors located at  $V_{00}, V_{11}$  and  $V_{12}$ . These three additional voltage space vectors are located at the midpoints of each side of the triangle  $[\Delta V_{01}V_{02}V_{03}]$  of equivalent 2-level inverter. Hence the  $[\Delta V_{01}V_{02}V_{03}]$  of 3-level inverter consists of four sectors, formed by the voltage space vectors located at  $V_{01}, V_{11}, V_{02}, V_{12}, V_{03}, V_{00}$ . Also the  $\Delta V_{01}V_{03}V_{04}$  contains another four sectors. So the total number of sectors in 3-level two legged inverter is 8 [S1-S8] as shown in Fig.3 (b).

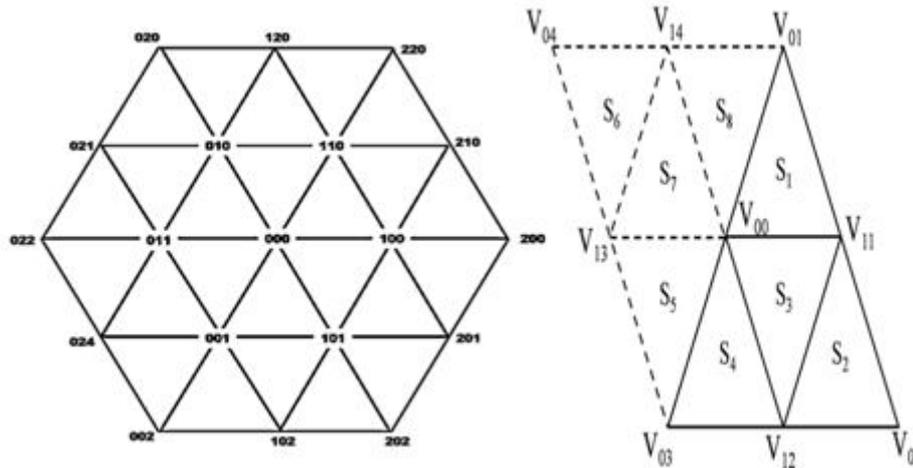


Fig. 3: Voltage space vector locations of (a) three legged 3-level inverter (b) two legged 3-level inverter

In this manner, each sectors formed by the voltage space vectors of 2-level inverter divided into four smaller sectors results the voltage space vector representation of 3-level inverter with 8 sectors.

The number of sectors for two legged 2-level and 3-level configurations are 2 and 8 respectively. The number of triangles for conventional three phase 2-level and 3-level configurations are 6 and 24 respectively. Generalizing the number of sectors,  $s$ , for two legged  $n$ -level inverter is,

$$s = 2 * (n - 1)^2 \tag{1}$$

Whereas the number of sectors for conventional three phase  $n$ -level inverter is,

$$s = 6 * (n - 1)^2 \tag{2}$$

where,  $n$  is the number of levels of the inverter.

Hence the number of sectors for two legged multilevel inverter is only one-third of the number of sectors for conventional multilevel inverters. The advantage of lesser number of sectors simplifies the space vector generation for higher level inverters.

In the case of two legged multilevel inverters, the voltage space vector representation of higher level inverters can be obtained simply by the repetitive division of each sector in the voltage space vector representation of the equivalent 2-level inverter. The voltage space vector representation of 2-level inverter grows to that of higher level inverters by repeated division of each sector. Switching voltage vectors and switching states of the multilevel inverters can be generated from the equivalent 2-level inverter by using repeated triangularization algorithm.

### III. SVPWM GENERATION FOR TWO LEGGED MULTILEVEL INVERTER

This section explains the steps for the implementation of SVPWM generation for two legged multilevel inverter. The generation of SVPWM for two legged multilevel inverter using proposed method involves the following steps: (i) Identification of equilateral triangle (sector) in which the tip of reference space vector lies (ii) Determination of the switching vectors and corresponding switching states (iii) Calculation of the duration of each of the switching voltage vectors.

#### A. Sector identification and determination of switching vector

Sector identification determines the triangle that encompasses the tip of the reference space vector. The vertices of the identified sector represent the locations of switching voltage space vectors which are used to synthesize the

reference space vector. Repeated triangularization algorithm is used for the sector identification. Consider three reference instantaneous phase voltages  $V_a$ ,  $V_b$  and  $V_c$ . Using coordinate transformation, three phase voltages are transformed in to  $(\alpha, \beta)$  plane. This can be obtained as,

$$V_\alpha = \frac{\sqrt{3}}{2} V_a \quad (3)$$

$$V_\beta = \frac{\sqrt{3}}{2} (V_b - V_c) \quad (4)$$

In order to identify the sector, first determine the location of the tip of the reference space vector OP from among the two regions of the equivalent 2-level inverter. In the previous sections, it is mentioned that the switching voltage representation of 2-level inverter contains two sectors (equilateral triangles), where sector I is formed by the vectors located at  $V_{01}$ ,  $V_{02}$ ,  $V_{03}$  and sector II is formed by the vectors located at  $V_{01}$ ,  $V_{03}$ ,  $V_{04}$ .  $\alpha$  and  $\beta$  coordinates of  $V_{01}$ ,  $V_{02}$ ,  $V_{03}$  and  $V_{04}$  for equivalent 2-level inverter are  $(1, \sqrt{3})$ ,  $(3, -\sqrt{3})$ ,  $(-1, -\sqrt{3})$  and  $(-3, \sqrt{3})$  as shown in Fig. 7(a). The switching states of  $V_{01}$ ,  $V_{02}$ ,  $V_{03}$  and  $V_{04}$  are also shown in Fig. 7(a) [in square brackets]. To identify the sector which encloses the tip of the reference space vector, compute the coordinates of the centroid of the both two equilateral triangles of the equivalent 2-level inverter. The coordinates of the centroid of the equilateral triangles can be determined by taking the average of the coordinates of the three vertices. The coordinates of the centroid  $(\alpha_c, \beta_c)$  for an equilateral triangle with three vertices having coordinates  $(\alpha_1, \beta_1)$ ,  $(\alpha_2, \beta_2)$  and  $(\alpha_3, \beta_3)$  is thus given by

$$\alpha_c = \frac{1}{3} (\alpha_1 + \alpha_2 + \alpha_3) \quad (5)$$

$$\beta_c = \frac{1}{3} (\beta_1 + \beta_2 + \beta_3) \quad (6)$$

Using these equations compute the coordinates of the centroid of the 2 sectors (equilateral triangles) of the equivalent 2-level inverter. The location of the tip of the reference space vector OP from among these triangular sectors are found by determining the sector whose centroid is closest to the tip of the reference space vector. Let  $(V_\alpha, V_\beta)$  be the coordinates of the tip of the reference space vector OP. The distance between the tip of the reference space vector and centroid of a sector is found by the following equation,

$$d = (\alpha_c - V_\alpha)^2 + (\beta_c - V_\beta)^2 \quad (7)$$

Compute the equation for both 2 sectors of the 2-level inverter and thus find the sector which encloses the tip of the reference space vector. In this case  $\Delta V_{01} V_{02} V_{03}$  is the triangular sector in which tip of the reference space vector lies as shown in Fig. 7(a). In the first application of triangularization algorithm to the region  $[\Delta V_{01} V_{02} V_{03}]$  which encloses the tip of the reference space vector, it gets divided into four equilateral triangles. Sector I of the equivalent 2-level inverter in which tip of the reference space vector lies undergoes first triangularization algorithm and generate three additional vectors  $V_{00}$ ,  $V_{11}$ ,  $V_{12}$  and gets divided in to four smaller triangular regions as in Fig. 7(b).

According to Triangularization algorithm, the average of  $\alpha$  and  $\beta$  coordinates of the voltage vectors at  $V_{01}$  and  $V_{02}$  will result in the coordinates of  $V_{11}$  as  $(2, 0)$ . The averaging applied to the switching states at  $V_{01}$  and  $V_{02}$  will result in the switching states corresponding to the switching vector located at as  $[4 \ 2 \ 2]$ . The voltage vectors and switching states of  $V_{12}$  and  $V_{00}$  are also computed similarly and are also shown in Fig. 7(b). Then again compute the centroid of the new four triangular sectors and from among these sectors find the region in which the tip of the reference space vector lies using the equations (5)-(7). It is found that the triangle which encloses the tip of the reference space vector OP is  $\Delta V_{00} V_{11} V_{12}$ .

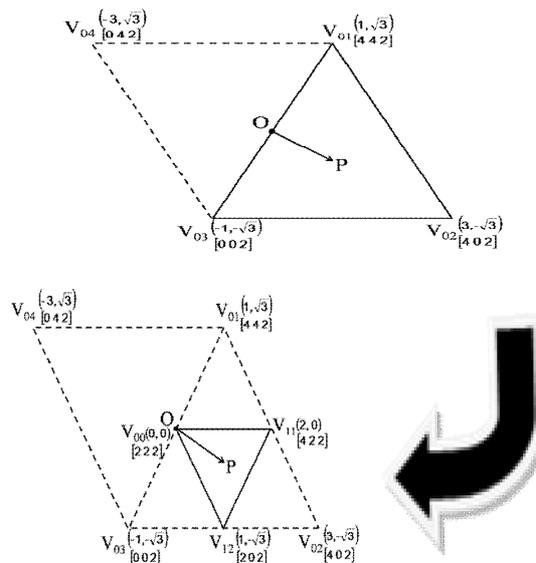


Fig. 7: Illustration of the proposed sector identification for a 3-level two legged inverter

Through repeated triangularization the sectors of any higher level inverter can be generated and through the proposed method sector identification and associated switching vectors are determined.

**B. Switching vector time calculation**

The procedure for identification of sector and determination of switching voltage vectors are explained in the above section. The next stage involves determining the duration for which the voltage space vectors located at the vertices of the identified sector are to be switched. Since one phase is clamped to a constant voltage, space vector representation of two legged multilevel inverter has unique zero vector. The switching time equation for a 3-level inverter is shown in Table I. From the time durations and associated switching vectors the actual gating signal durations are computed using simple addition operation.

TABLE I

SWITCHING TIME EQUATIONS FOR 3-LEVEL INVERTER

Sector	T <sub>1</sub>	T <sub>2</sub>
S <sub>1</sub>	$\left[ 2V_z - \frac{2}{\sqrt{3}} V_F \right] T_s$	$\frac{4}{\sqrt{3}} V_F T_s$
S <sub>2</sub>	$\left[ 2V_z - \frac{2}{\sqrt{3}} V_F - 1 \right] T_s$	$\left[ \frac{4}{\sqrt{3}} V_F + 1 \right] T_s$
S <sub>3</sub>	$\left[ -2V_z + \frac{2}{\sqrt{3}} V_F + 1 \right] T_s$	$\left[ 2V_z + \frac{2}{\sqrt{3}} V_F \right] T_s$
S <sub>4</sub>	$\left[ 2V_z - \frac{2}{\sqrt{3}} V_F \right] T_s$	$\left[ \frac{4}{\sqrt{3}} V_F T_s + 1 \right]$
S <sub>5</sub>	$\left[ -2V_z + \frac{2}{\sqrt{3}} V_F \right] T_s$	$\left[ 2V_z + \frac{2}{\sqrt{3}} V_F + 1 \right] T_s$

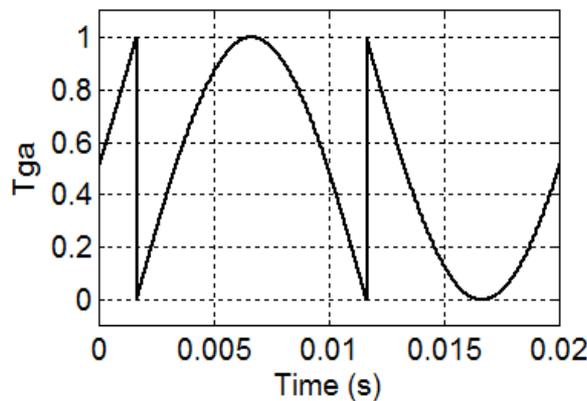
$S_6$	$\left[ -2V_L + \frac{2}{\sqrt{3}} V_{\beta} - 1 \right] T_s$	$\left[ 2V_L + \frac{2}{\sqrt{3}} V_{\beta} + 1 \right] T_s$
$S_7$	$\left[ 2V_L - \frac{2}{\sqrt{3}} V_{\beta} + 1 \right] T_s$	$\frac{4}{\sqrt{3}} V_{\beta} T_s$
$S_8$	$\left[ -2V_L + \frac{2}{\sqrt{3}} V_{\beta} \right] T_s$	$\left[ 2V_L + \frac{2}{\sqrt{3}} V_{\beta} \right] T_s$

#### IV. SIMULATION RESULTS

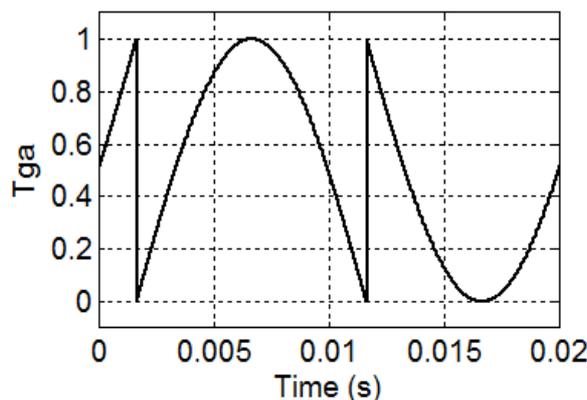
To verify the validity of the proposed algorithm for generation of SVPWM, simulation is carried out in MATLAB/SIMULINK for two legged three phase inverter fed Permanent Magnet Synchronous Motor (PMSM) drive with a DC link voltage of 400V. Fig. 8 presents the simulation results of two legged inverter for 3-level configuration with phase C clamped to 200V. The parameters of the motor are given in Appendix. Fig. 8(a) shows the gating signal waveform for 3-level and 5-level operations.

The pole voltage for the 3-level operation ( $V_{a0}$ ) is shown in Fig. 8(b) and the inverter switches between the levels of 150V, 200V and 250V. The phase voltage and current when 3-level inverter simulated with permanent magnet synchronous motor are shown in Fig. 8(c) and Fig.8(d) respectively.

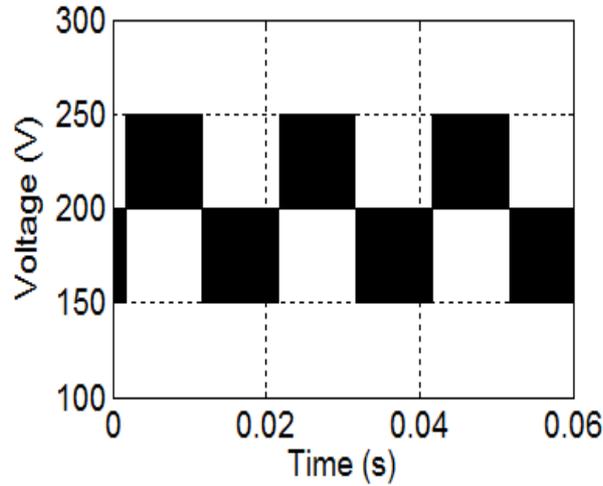
For 3-Level configuration



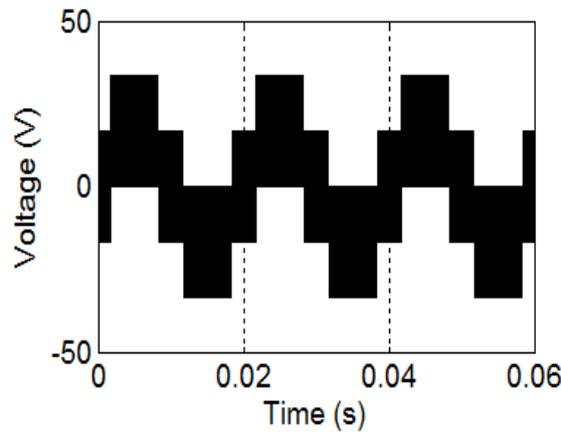
(a) Gating signal waveform



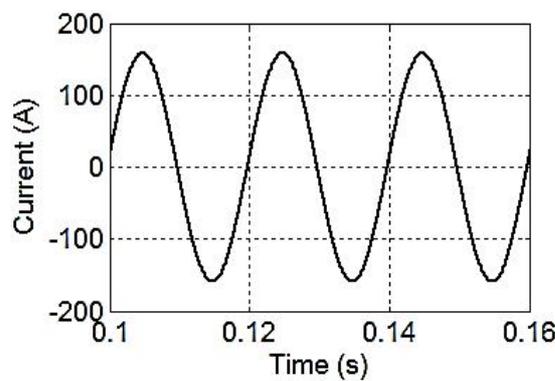
(b) Gating signal waveform



(c) Pole Voltage waveform corresponding to 400V operation



(d) Phase Voltage waveform for the PMSM motor



(e) PMSM current waveform

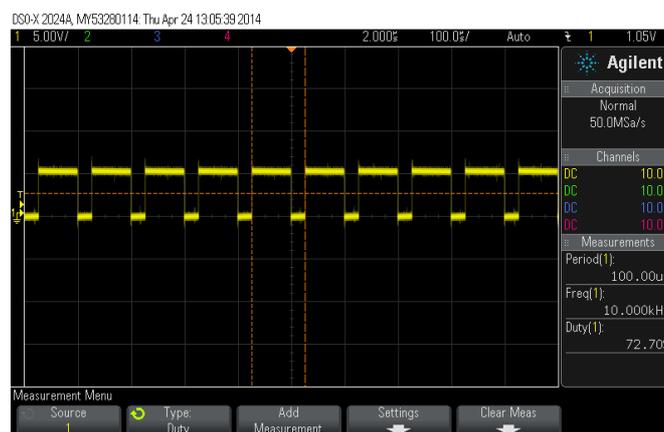
Fig. 8: Simulation results of two legged inverter (3-level configuration)

### V. EXPERIMENTAL RESULTS

BLDC motor control is implemented using 24HJ128GP310 microcontroller. PWM pulses for the MOSFET switches in the 3 phase bridge inverter driven by IR2110 driver circuit are generated by the microcontroller. Lookup table formulated depending upon the Hall signals, PWM and dead band is implemented. Control algorithm is implemented by Assembly language programming in microcontroller. MPLAB IDE v 8.92 tool of MICROCHIP has been write the code in assembly language using PIC24H family data sheet. The experimental validation setup is shown in Fig.9.



Fig. 9: Experimental Setup of two legged inverter (3-level configuration)



(a)

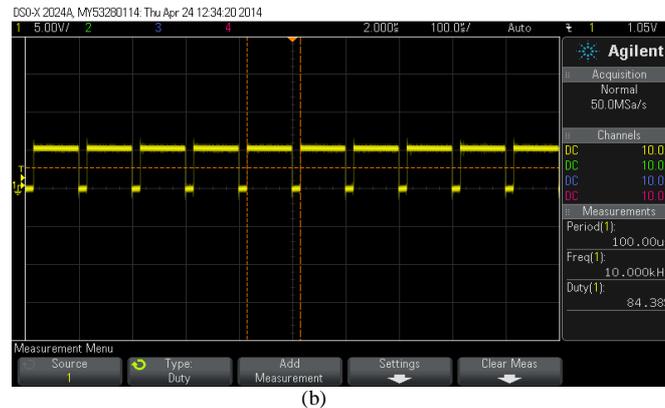


Fig. 9: Experimental results of two legged inverter

## VI. CONCLUSIONS

This paper presents the voltage representation of the two legged multilevel inverter. The proposed work involves triangularization algorithm for the generation of the SVPWM and thus it simplify the implementation process. No need of look up table for the sector identification. The basic unit of the fractal structure of the two legged multilevel inverter is the triangle and each triangle is undergoes repeated division for higher level inverters. The implementation result is explained for 3-level inverter and simulation results are presented for 3-level inverter configurations. The proposed work can be easily extended for higher level two legged inverters. The validation of the algorithm through simulations in MATLAB/SIMULINK and experimental in PIC24HJ128GP310 microcontroller has been carried out for 3-level inverter configurations.

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## International Journal of Innovative Research in Science, Engineering and Technology

An ISO 3297: 2007 Certified Organization

Volume 3, Special Issue 5, July 2014

### International Conference On Innovations & Advances In Science, Engineering And Technology [IC - IASET 2014]

Organized by

**Toc H Institute of Science & Technology, Arakunnam, Kerala, India during 16th - 18th July -2014**

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